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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,974	12/02/2003	Santosh Savekar	15148US02	4960

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EXAMINER	
TAYONG, HELENE E	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,974	SAVEKAR ET AL.	
	Examiner	Art Unit	
	Helene E. Tayong	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/31/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/31/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1- 4, 6-9 and 11- 21 are rejected under 35 U.S.C. 102 (e) as being anticipated by Jiang et al (US patent 6,614441)

(1) regarding claim 1:

Jiang teaches a system (Fig 1,2) for displaying images on a display comprising :

a decoder (fig 1,180, fig. 2, 200, fig. 5, 530) for decoding encoded images (col 4, lines 13-15) and parameters associated with the images (530, col. 9, lines 61-65)

image buffers (160) for storing the decoded images (col. 5, lines 5-9);

parameter buffers (interpreted as registers 310-330, fig 3) for storing the decoded parameters associated with the decoded images (col. 6, lines 57-60);

and a display manager "monitor" (150, fig 1) for determining when to overwrite an existing image in the image buffers (auto-flip mechanism) (col. 6, lines 45-51), and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer (col. 6, lines 45-11);

and wherein the decoder (200, video capture engine) overwrites the existing image after receiving the signal (col. 5, lines 29-36).

(2) regarding claim 2;

wherein the set of parameters (interpreted as FFF, RFF) includes a parameter indicating when the system is utilizing a technique requiring selective images to be displayed more than once (col. 9, 54-61).

(3) regarding claim 3;

wherein the system for displaying images on a display (100, Figure 1) further comprises:

a first processor (interpreted as video stream decoder, 180, fig 1);

a second processor (interpreted as Graphics controller, 140, fig 1);

a first memory (DRAM,190, fig. 1);

a second memory (interpreted as system memory, 130 fig. 1); and

wherein the first memory(190) stores an instruction set

for the decoder (col 4, lines 8-11).

(4) regarding claim 4;

wherein the first processor (180) executes the instruction for the decoder (col. 4, lines 14-16).

(5) regarding claim 6;

wherein the second processor (fig.6., 224, col. 11, lines 44-46) determines when to overwrite the existing image.

(6) regarding claims 7;

wherein an integrated circuit (fig. 6) comprises the first processor(200) and first memory(260), and wherein the second processor(220) is off-chip from the integrated circuit (col. 9, lines 44-47).

(7) regarding claim 8;

where the second memory is an off-chip memory (interpreted as system memory or main memory, 130, fig 1) (col. 3, lines 21-25).

(8) regarding claim 9;

wherein the first memory is a SRAM (SRAM is interpreted as any kind of RAM, col. 4, lines 11-14)

(9) regarding claim 11;

the second memory stores the image buffers (col. 3, lines 42-46).

(10) regarding claim 12;

wherein the second memory stores the parameter buffers (col. 6, lines 57-63).

(11) regarding claim 13;

a first processor (180, col. 9, lines 14-17); and

a first memory connected to the processor (col. 9, lines 22-26), the first memory storing instructions, wherein execution of the instructions by the first processor causes:

decoding images (col 9,lines 26-31) ; and

overwriting an existing image after the processor receives a signal indicating when to overwrite the existing image (col. 10, lines , 13-20).

(12) regarding claim 14;

wherein execution of the instructions by the first processor further causes:

displaying the images (col. 9, lines 19-22).

(13) regarding claim 15;

a second processor (140) connected to the integrated

circuit (col. 4, lines 35-41);

a second memory (130) connected the processor (140), the

second memory (RAM) storing instructions, wherein execution of the

instructions by the second processor (140) causes:

determining when to .overwrite the existing frame (col 5, lines 59-61);

and transmitting signal the first processor indicating when overwrite the existing

frame (col. 5, lines 61-65).

(14) regarding claim 16;

wherein execution of the instructions of the first memory (190) by the first

processor further causes:

decoding parameters associated with the images.

(15) regarding claim 17;

examining some of the decoded parameters (TFF,RFF) associated with the

images by the second processor (140) (clo.10, lines 1-4).

(16) regarding claim 18;

The circuit of claim 16, further comprising

parameter buffer (register) connected the integrated circuit and a

frame buffer (160, fig 1) connected the integrated circuit (100, fig. 1),

wherein the parameter buffer stores the decoded parameters ((col. 6, lines 56-62), and the frame buffer stores the decoded images (col. 5, lines 40-42).

(17) regarding claim 19;

decoding images (col.5, lines 5-11);

decoding parameters associated with the images (col. 9, lines 61-65);

overwriting an existing buffered decoded image (col. 5, lines 59-61) ; and

displaying the decoded images(col. 5, lines 60-61).

(18) regarding claim 20;

determining when to overwrite the existing image (col. 5, lines 60-61);

and transmitting a signal indicating when to overwrite

the existing image (col. 5, lines 61-65).

(19) regarding claim 21;

decoding parameters associated with the images (col. 9, lines 61-65);

and examining some of the decoded parameters associated with the images (col. 10, lines 5-8);

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al (6614441) in view of Savekar et al (7133046)

(1) regarding claim 5;

Jiang et al. further discloses a hardware-based graphics for processing video data in a computer system (col. 1, line1-2 to col. 2, lines 1)

Jiang et al. discloses all of the subject matter as described above except for specifically teaching that the second memory stores an instruction set for the display manager, the instruction set for the display manager executed by the second processor.

However, Savekar et al in the same field of endeavor, teaches that the second memory(DRAM) stores an instruction set for the display manager, the instruction set for the display manager(311) executed by the second processor (307) (col. 8, lines 38-48).

One of ordinary skill in the art would have clearly recognized that storing the instruction sets for the display manager in the secondary memory would help increases memory bandwidth .To increase the efficiency of low memory usage, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the second memory of Jiang et al. with the memory of Savekar et al.

(2) regarding claim 10;

Jiang et al. further discloses a hardware-based graphics for processing video data in a computer system (col. 1, line1-2 to col. 2, lines 1)

Jiang et al. discloses all of the subject matter as described above except for specifically teaching that the second memory is a DRAM.

However, Savekar et al. in the same field of endeavor, teaches that the second memory is DRAM (col. 7, lines 1-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the second memory DRAM by Savekar et al. for storage because it is less costly and increased speed.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jiang et al.(US patent number 6614441) discloses a method and mechanism of automatic video buffer flipping and display sequence management

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helene E. Tayong whose telephone number is (571) 270-1675. The examiner can normally be reached on Monday - Friday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Liu Shuwang can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helene Tayong
1/18/07

SHUWANG LIU
SUPERVISORY PATENT EXAMINER